Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (currently amended) A memory device[[,]] comprising:

a plurality of memory cells, each memory cell includes first and second ports forming a memory array with first and second access ports, wherein the first access port is an external port for read and write memory accesses and the second access port is an internal port for refresh operations;

~~a memory cell array having a multitude of memory cells, first and second bitlines, and first and second wordlines, each of said memory cells being coupled to one of said first bitlines, one of said second bitlines, one of said first wordlines, and one of said second wordlines;~~

~~each of said memory cells being accessible through one of said first wordlines and one of said first bitlines by an external port and being accessible through one of said second wordlines and one of said second bitlines by an internal port;~~

~~said external port being connected to input terminals to receive input signals in order to select one of said memory cells for an external data access;~~

a refresh control unit generating refresh control signals to control refreshing of the memory cells ~~through said internal port~~; and

a contention detection circuit, ~~said contention detection circuit~~, the contention detection circuit, when a memory access via the external port and a refresh operation via the internal port occur, compares an access row address of the memory access with a refresh row address of the

refresh operation and suppressing the refresh operation if the access address and the refresh row address are equal ~~receiving a row address in response to an external read or write access through said external port and receiving a refresh address for a row of memory cells to be refreshed, said contention detection circuit suppressing a refresh, if said refresh address equals said row address~~.

2. (currently amended) ~~The~~ A memory device ~~according to claim 1,~~ comprising:

a memory cell array having a multitude of memory cells, first and second bitlines, and first and second wordlines, each of said memory cells being coupled to one of said first bitlines, one of said second bitlines, one of said first wordlines, and one of said second wordlines;

each of said memory cells being accessible through one of said first wordlines and one of said first bitlines by an external port and being accessible through one of said second wordlines and one of said second bitlines by an internal port;

said external port being connected to input terminals to receive input signals in order to select one of said memory cells for an external data access;

a refresh control unit generating refresh control signals to control refreshing of the memory cells through said internal port;

a contention detection circuit, said contention detection circuit receiving a row address in response to an external read or write access through said external port and receiving a refresh address for a row of memory cells to be refreshed, said contention detection circuit suppressing a refresh, if said refresh address equals said row address; and

wherein each one of said memory cells comprises[[:]]

a first selection transistor coupled to one of said first wordlines and one of said first bitlines[[;]],

a second selection transistor coupled to one said second wordlines and one of said second bitlines[[;]], and

a storage node connected to said first selection transistor and said second selection transistor.

3. (currently amended) The memory device according to claim 2[[,]] wherein each one of said memory cells comprises:

a storage transistor having a drain/source path and a gate terminal, said drain/source path being connected to said first and said second selection transistors; and

said gate terminal being connected to a reference potential.

4. (currently amended) The memory device according to claim 2 [[1,]] wherein said external port is connected to input terminals designed to receive one of an address signal, a signal determining a read or a write operation, a data clock signal, and a device select signal.

5. (currently amended) The memory device according to claim 4[[,]] wherein said internal port is hidden from said address signal, said signal determining a read or a write operation, and said device select signal.

6. (currently amended) The memory device according to claim 2 [[1,]] comprising:

a first bank of sense amplifiers, wherein each one of said first bitlines is connected to one of said sense amplifiers of said first bank;

a column decoder, wherein an individual one of said sense amplifiers of said first bank can be selected to perform one of data read to an external terminal; and

data write from an external terminal.

7. (currently amended) The memory device according to claim 6[[,]] comprising:

a second bank of sense amplifiers, wherein each one of said second bitlines is connected to one of said sense amplifiers of said second bank, and wherein multiple of said amplifiers are selected to perform a refresh of a row of memory cells.

8. (currently amended) The memory device according to claims 2 [[1,[] comprising:

a first clock terminal to receive a system clock signal to synchronize external data input and output;

a second clock terminal to receive a reference clock signal; and

a synchronization circuit to output a refresh clock signal which is synchronized to one of said system clock or said reference clock signals.

9. (currently amended) The memory device according to claim 8[[,]] comprising:

a refresh address counter to generate row addresses of rows of memory cells to be refreshed, said address counter being controlled by said refresh clock.

10. (previously presented) The memory device according to claim 8 wherein said memory cell array comprises at least two blocks of memory cells, said blocks being provided with a refresh row address in parallel, said refresh control circuit generating a separate refresh enable signal for each of said blocks to perform a refresh operation for one of said blocks subsequent to a refresh operation for another one of said blocks.

11. (cancelled)

12. (currently amended) A memory device[[,]] comprising:

a memory cell array having memory cells, each of said memory cells being accessible through a first port and through a second port, only said first port of said first and second ports being accessible by an external address signal to select one of said memory cells; and

a refresh control circuit designed to generate refresh control signals to refresh said memory cells through said second port, wherein said refresh control circuit receives a system clock signal and a reference clock signal, said refresh control circuit has a refresh address counter to provide a sequence of addresses for subsets of memory cells to be refreshed, said memory device having a normal mode and a power-down mode, wherein said refresh address

counter is controlled by said system clock signal during the normal mode and is controlled by said reference clock signal during the power-down mode; and

a contention detection circuit receiving ~~a~~ an internal or refresh address to access a subset of said memory cells for a refresh operation and an external address to access at least of one said memory cells ~~of said subset of memory cells~~ for a ~~an external~~ read or write operation, said contention detection circuit suppressing a refresh operation for said subset of said memory cells if the external address accesses a memory cell within the subset of memory cells of the refresh address.

13. (cancelled)

14. (previously presented) The memory device according to claim 12 wherein a refresh operation is performed for another subset of memory cells.

15. (previously presented) The memory device according to claim 12 wherein said subset of memory cells is a row of memory cells.

16. (currently amended) The memory device according to claim 12[[,]] wherein said refresh control circuit receives a system clock signal and a reference clock signal, said refresh control circuit has a refresh address counter to provide a sequence of addresses for subsets of memory cells to be refreshed, said memory device having a normal mode and a power-down

mode, wherein said refresh address counter is controlled by said system clock signal during the normal mode and is controlled by said reference clock signal during the power-down mode.

17. (currently amended) The memory device according to claim 12 ~~16,~~ wherein said refresh control circuit comprises a synchronization circuit that synchronizes a clock signal to one of said system clock or reference clock signals in response to one of said normal or power-down modes, wherein said clock signal controls said refresh address counter.

18. (currently amended) The memory device according to claim 12 ~~16,~~ wherein said reference clock signal has a lower frequency than said system clock signal.

19. (currently amended) The memory device according to claim 12[[,]] wherein each one of said memory cells comprises:

a first selection transistor coupled to one of said first wordlines and one of said first bitlines and a second selection transistor coupled to one said second wordlines and one of said second bitlines; and

a storage node connected to said first selection transistor and said second selection transistor.

20. (currently amended) The ~~A~~ memory device[[,]] of claim 12 wherein ~~comprising~~:

~~a memory cell array having a multitude of~~ the memory cells are arranged in rows;

a first row decoder to activate one of said rows in response to ~~an~~ the external address; and

a second row decoder to activate one of said rows in response to an internal address generated by the refresh control circuit; ~~and~~

~~a refresh control circuit to refresh the memory cells of a row which is activated by said second row decoder~~.

21. (cancelled)

22. (currently amended) The memory device according to claim 20[[,]] wherein each one of said memory cells comprises a first selection transistor connected to the first row decoder through a first wordline and a second selection transistor connected to the second row decoder through another wordline and a storage node coupled to the first and the second selection transistors.

23. (currently amended) An integrated circuit (IC) comprising:

a multi-port memory cell array having at least first and second ports;

a plurality of memory cells accessible by the first and second ports;

a refresh control unit generating refresh control signals to control refreshing of the memory cells ~~through one of the ports~~; and

a contention detection circuit to for detecting contention between a refresh operations from one of the ports and a read or write memory access operations from other of the ports and suppressing the refresh~~ing~~ operation when contention occurs to allow the read or write memory access to execute.

24. (currently amended) The IC of claim 23 wherein ~~one of~~ the first ports comprises an internal access port for performing refreshing of the memory cells ~~operations~~ and the second ~~other one of the~~ ports comprises an external port for performing read and write memory access operations.

25. (previously presented) The IC of claim 24 wherein:

refresh control signals include a refresh address indicating location of a subgroup of memory cells of the array to be refreshed address for refreshing a subgroup of memory cells of the array; and

the contention suppressing refreshing operation when the memory access operation accesses a memory cell within the subgroup of memory cells to be refreshed.

26. (previously presented) The IC of claim 25 wherein the subgroup of memory cells comprises at least one row of memory cells.

27. (previously presented) The IC of claim 25 wherein the subgroup of memory cells comprises a row of memory cells.

28. (previously presented) The IC of claim 23 wherein:

refresh control signals include a refresh address indicating location of a subgroup of memory cells of the array to be refreshed address for refreshing a subgroup of memory cells of the array; and

the contention suppressing refreshing operation when the memory access operation accesses a memory cell within the subgroup of memory cells to be refreshed.

29. (previously presented) The IC of claim 28 wherein the subgroup of memory cells comprises at least one row of memory cells.

30. (currently amended) The IC of claim 23 ~~28~~ wherein ~~the subgroup of memory cells comprises at a row of memory cells~~ the refresh control circuit comprises a refresh address counter in the refresh control circuit for generating refresh control signals corresponding address of memory cells to be refreshed.

31. (currently amended) The IC of claim 30 ~~23 wherein the refresh control circuit comprises a refresh address counter in the refresh control circuit for generating refresh control signals corresponding address of memory cells to be refreshed~~ wherein the address of memory cells to be refreshed comprises the address of a row of memory cells to be refreshed.

32. (currently amended) The IC of claim 23 ~~31~~ wherein a system clock signal and a reference clock signal are provided to the refresh control circuit, the system clock signal controls the refresh address counter when the memory array is operating in a normal mode of operation and the reference clock signal controls the refresh address counter when the memory array is in a power-down or reduced power mode of operation.

33. (previously presented) The IC of claim 32 wherein the reference clock signal has a lower frequency than the system clock signal.

34. (previously presented) The IC of claim 32 wherein the refresh control circuit comprises a synchronization circuit that synchronizes a clock signal to one of the system or reference clock signals depending on the mode of operation of the memory array.

35. (previously presented) The IC of claim 34 wherein the reference clock signal has a lower frequency than the system clock signal.

36. (new) The IC of claim 23 wherein a system clock signal and a reference clock signal are provided to the refresh control circuit, the system clock signal controls the refresh address counter when the memory array is operating in a normal mode of operation and the reference clock signal controls the refresh address counter when the memory array is in a power-down or reduced power mode of operation.

37. (new) The IC of claim 36 wherein the reference clock signal has a lower frequency than the system clock signal.

38. (new) The IC of claim 36 wherein the refresh control circuit comprises a synchronization circuit that synchronizes a clock signal to one of the system or reference clock signals depending on the mode of operation of the memory array.

39. (new) The IC of claim 38 wherein the reference clock signal has a lower frequency than the system clock signal.

40. (new) An IC comprising:

a plurality of memory cells forming a memory array arranged in rows and columns;

a refresh control unit generating refresh control signals to control refreshing of the memory cells; and

a contention detection circuit, when a read or write memory access and a refresh operation are to the same row, suppresses the refresh operation to enable execution of the read or write memory access.

41. (new) The IC of claim 40 wherein the memory cells comprise first and second ports, wherein the read or write memory access is to one of the first and second ports and the refresh operation is to other of the first and second ports.